Features

- Demonstrates recommended layout and grounding arrangements
- CS8406 generates S/PDIF, and EIAJ-340 compatible digital audio
- Requires only an analog signal source and power supplies for a complete Analog-to-Digital-Converter system

Description

The CDB5361 evaluation board is an excellent means for quickly evaluating the CS5361 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog signal source, and a power supply.

Also included is a CS8406 digital audio interface transmitter which generates S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

ORDERING INFORMATION

CDB5361 Evaluation Board
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1. CDB5361 SYSTEM OVERVIEW
The CDB5361 evaluation board is an excellent means of quickly evaluating the CS5361. The CS8406 digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment.

The CDB5361 schematic has been partitioned into 7 schematics shown in Figure 2 through Figure 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS8406 DIGITAL AUDIO TRANSMITTER
The system generates and encodes standard S/PDIF data using a CS8406 Digital Audio Transmitter (See Figure 6). The outputs of the CS8406 are RS422 compatible differential line drivers. The CS8406 supports both Left Justified and I2S data formats, as determined by the DIP switch, S2. A description of the CS8406 is included in the CS8406 datasheet.

3. INPUT/OUTPUT FOR CLOCKS AND DATA
The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, J13. The schematic for the clock/data input/output is shown in Figure 5.

The CDB5361 allows some flexibility as to the generation of the clocks. When the CS5361 and CS8406 are in slave mode, the SCLK and LRCK must be provided via the header, J13. MCLK must be generated from the on board oscillator, Y1. This oscillator is socketed to allow other frequency oscillators to be used.

4. POWER SUPPLY CIRCUITRY
Power is supplied to the evaluation board by six binding posts (-12V, +12V, VD, VL, GND, +5 V), see Figure 8. -12V and +12V supply the input amplifiers while the VD input supplies the VD pin of the CS5361. VL supplies power to the VL pin of the CS5361 and to the level shifter circuits. The +5 V input supplies power to the +5 V digital circuitry and the VA pin of the CS5361.

5. GROUNDING AND POWER SUPPLY DECOUPLING
The CS5361 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 details the power distribution used on this board. The decoupling capacitors are located as close to the CS5361 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. ANALOG INPUT FILTER
The CDB5361 implements a fully differential analog input buffer, as shown in Figure 2. Note that there is no attenuation associated with the input buffer, so a 2Vrms differential input applied at the XLR connectors will provide a full-scale 2Vrms differential input to the CS5361.
## Table 1. System Connections

<table>
<thead>
<tr>
<th>CONNECTOR</th>
<th>INPUT/OUTPUT</th>
<th>SIGNAL PRESENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>-12V</td>
<td>Input</td>
<td>-12V power for the input op-amps</td>
</tr>
<tr>
<td>+12V</td>
<td>Input</td>
<td>+12V power for the input op-amps</td>
</tr>
<tr>
<td>VD</td>
<td>Input</td>
<td>+3.3V to +5V power for the CS5361</td>
</tr>
<tr>
<td>VL</td>
<td>Input</td>
<td>+2.5V to +5V power for the CS5361</td>
</tr>
<tr>
<td>GND</td>
<td>Input</td>
<td>Ground connection from power supply</td>
</tr>
<tr>
<td>+5V</td>
<td>Input</td>
<td>+ 5 Volt power</td>
</tr>
<tr>
<td>AINL</td>
<td>Input</td>
<td>Differential analog input left channel</td>
</tr>
<tr>
<td>AINR</td>
<td>Input</td>
<td>Differential analog input right channel</td>
</tr>
<tr>
<td>Optical Output</td>
<td>Output</td>
<td>Digital audio output</td>
</tr>
<tr>
<td>Coax Output</td>
<td>Output</td>
<td>Digital audio output</td>
</tr>
</tbody>
</table>

## Table 2. CDB5361 Jumper and Switch Settings

<table>
<thead>
<tr>
<th>JUMPER/SWITCH</th>
<th>PURPOSE</th>
<th>POSITION</th>
<th>FUNCTION SELECTED</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7</td>
<td>VD Power Source</td>
<td>ADJ *+3.3V +5V</td>
<td>Power from the Binding Post (J3) Power from the +3.3V Regulator Power from the +5V Supply</td>
</tr>
<tr>
<td>J8</td>
<td>VL Power Source</td>
<td>ADJ *+3.3V +5V</td>
<td>Power from the Binding Post (J4) Power from the +3.3V Regulator Power from the +5V Supply</td>
</tr>
<tr>
<td>J13</td>
<td>Input/Output for clocks/data</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>S1</td>
<td>Reset for the CDB5361</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>S2</td>
<td>CDB5361 Configuration</td>
<td>M1/M0 Open *Closed</td>
<td>Hi Low ADC *Open Closed</td>
</tr>
</tbody>
</table>

* denotes default factory settings
Figure 1. System Block Diagram and Signal Flow

- CS4406 Digital Audio Interface (Fig. 6)
- Level Shifter (Fig. 4)
- Crystal Oscillator (Fig. 7)
- Reset Circuit (Fig. 7)
- Differential Analog Input (Fig. 2)
- Clocks and Data Input (Fig. 5)

Legend:
- Solid lines represent signal flow.
- Arrows indicate direction of data flow.
Figure 2. Differential Analog Audio Input

CS5361:
R9, R13, R24, R28 equal 0 ohm
R16, R19 are not installed
Figure 4. Level Shifters
Figure 5. I/O for Clocks/Data

Figure 6. CS8406 Digital Audio Interface
Figure 7. Reset Circuit
Figure 8. Power Circuit
Figure 10. Top Layer
Figure 11. Bottom Layer