
CS4282P-CODEC Schematic Layout Guidelines

Introduction

This document describes the schematic and layout guidelines for the CS4282P High Performance 2CH Audio CODEC.

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1 Recommended External Components

1.1 CS4282P Typical Connection Diagram

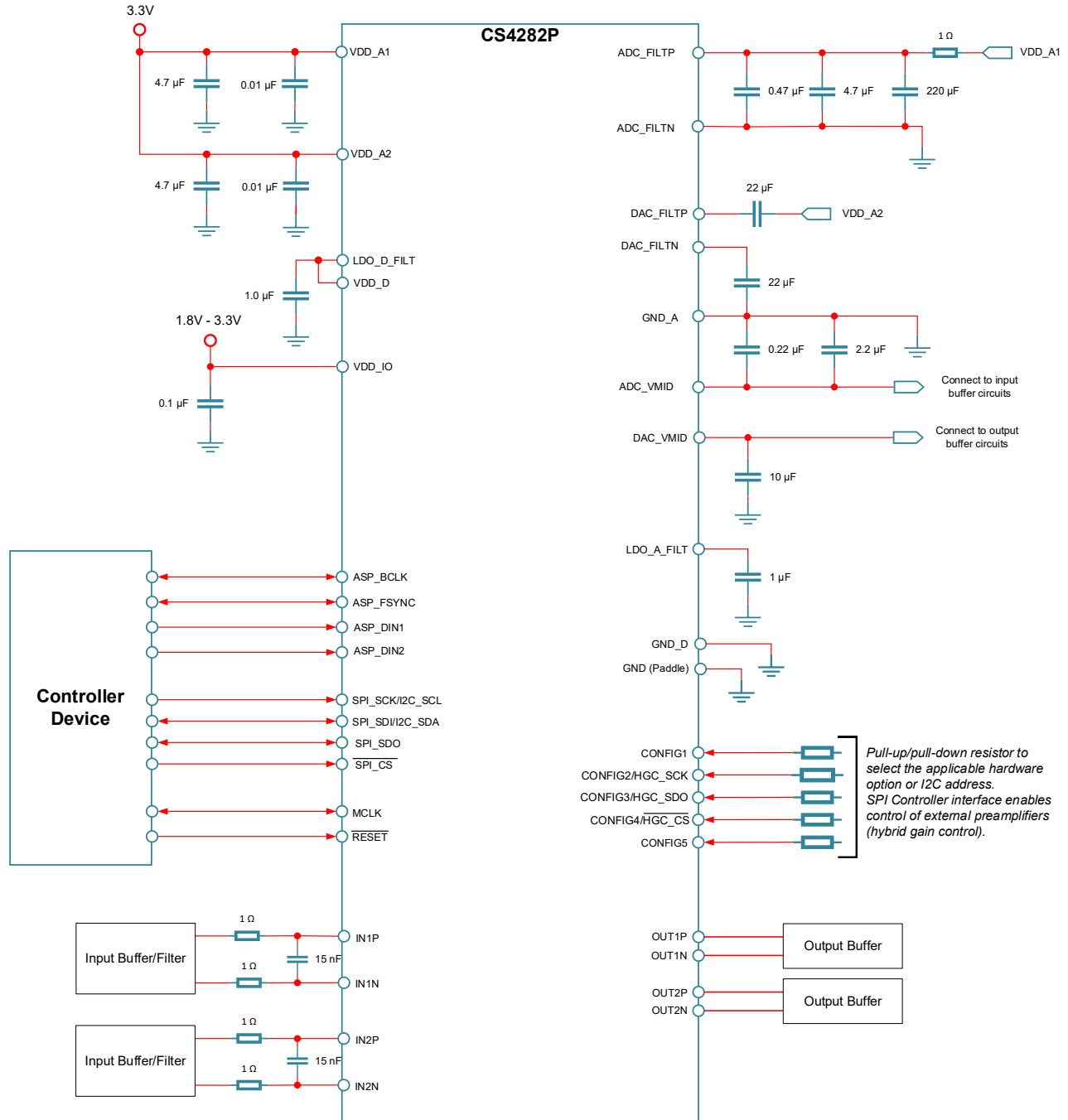


Figure 1: Connection Diagram

1.2 I2C Pull-Up

The I2C interface requires pull-up resistor to the VDD_IO supply. The pull-up resistor value is determined by the following factors.

- Bus capacitance
- Minimum I2C drive strength of ICs on the I2C bus

Cirrus Logic recommends the I2C pull-up resistors should be between 2.2k Ω and 10k Ω .

Table 1: Recommended i2c Pull-up Resistors

	Min	Typ	Max	Units
I2C pull-up resistors		2.2k to 10k		Ω

1.3 Reset Pull-Up

An optional pull-up resistor to VDD_IO (or pull-down to GND) is only required when the AP/MCU GPIO is unable to drive RESET at all times while the device is powered.

1.4 LDO_A_FILT

The LDO_A_FILT decoupling capacitor must not de-rate to a value less than 0.8 μ F at 1.8V applied to it.

Table 2: LDO_A_FILT Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
1.0 μ F	1.8V	0.8			μ F

1.5 LDO_D_FILT

The LDO_D_FILT decoupling capacitor must not de-rate to a value less than 0.8 μ F at 1.2V applied to it.

Table 3: LDO_D_FILT Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
1.0 μ F	1.2V	0.8			μ F

1.6 DAC_VMID

The DAC_VMID decoupling capacitors should not derate less than minimum value shown in the table below:

Table 4: DAC_VMID Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
10 μ F	1.65V	5			μ F

DAC_VMID has a maximum output current of 10 μ A. If the output current (arising from capacitor leakage and the input-buffer circuit) exceeds the maximum output current of the DAC_VMID pin, then an external VMID buffer is required.

1.7 DAC_FILT

The DAC_FILT decoupling capacitors should not derate less than the minimum value shown in the table below:

Table 5: DAC_FILT Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
22 μ F	3.3V	6.8			μ F

1.8 ADC_VMID

The ADC_VMID decoupling capacitors should not derate less than the minimum value shown in the table below:

Table 6: ADC_VMID Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
0.22 μ F	1.65V	0.1			μ F
2.2 μ F	1.65V	1.0			μ F

ADC_VMID has a maximum output current of 10 μ A. If the output current (arising from capacitor leakage and the input-buffer circuit) exceeds the maximum output current of the ADC_VMID pin, then an external VMID buffer is required.

1.9 ADC_FILT

The ADC_FILT decoupling capacitors should not derate less than the minimum value shown in the table below:

Table 7: ADC_FILTP Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
0.47 μ F	3.3V	0.22			μ F
4.7 μ F	3.3V	2.2			μ F

The 220 μ F electrolytic decoupling capacitor on ADC_FILT is a bulk capacitor for the ADC reference. The value of this capacitor can be reduced; however, this will increase the low frequency THD of the ADC.

1.10 Input Buffer Circuit

The analog input channels are supported using external buffer circuits. A typical buffer circuit is shown in **Figure 2**, comprising a high-pass filter and anti-alias filter. The typical buffer circuit shown produces a full-scale (0 dBFS) output from a 8 VRMS differential input.

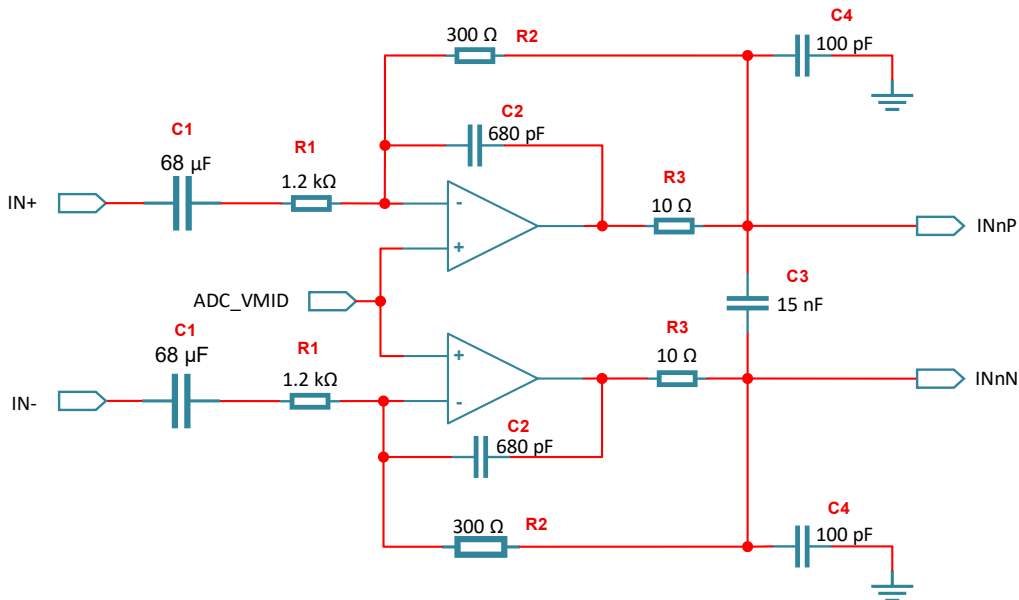


Figure 2: Differential Input Buffer

The high-pass filter is provided by the AC-coupling capacitor C1 and series resistor R1. Using the values shown, the –3 dB cut-off frequency (F_c) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1200 \times (68 \times 10^{-6})} = 1.95 \text{ Hz}$$

The anti-alias filter is provided by the op-amp and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides a –3 dB cut-off frequency around 640 kHz, suitable for the highest CS4282P sample rate of 768 kHz. The attenuation slope of –12 dB/octave results in 42 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The –3 dB cut-off frequency is approximated by the following equation:

$$F_c = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 2(C_3 + C_4)}} = \frac{1}{2\pi \sqrt{300 \times 10 \times 680 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 640 \text{ kHz}$$

The gain of the input buffer is determined by the ratio R_1/R_2 . The gain should be configured to provide a full-scale signal of 2 V_{RMS} at the input to the CS4282P. The values shown in Figure 2 provide a ratio of 4; in this configuration, the buffer supports a full-scale input of 8 V_{RMS} .

The VMID reference (common-mode level) for the input buffer can be provided from the ADC_VMID output. If the total input bias current for the all the op-amps attached to ADC_VMID is greater than 10μA, an external buffer is required to buffer the ADC_VMID voltage, as shown in Figure 3.

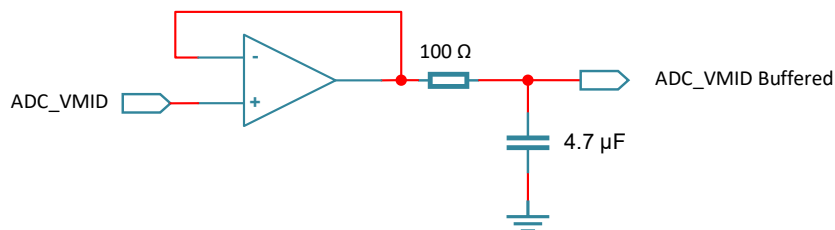


Figure 3 Example ADC_VMID Buffer Circuit

1.10.1 Unused Input Pins

The recommended input buffer circuit (see Figure 2) provides a differential connection to the input pins INxP and INxN. Alternative input-buffer circuits may use only a single-ended connection to INxP or INxN. If a single-ended input configuration is used, the unused input pin must be connected to a buffered VMID reference. See Error! Reference source not found. for a buffered VMID circuit. If one or more input channel is not used (disabled), the respective input pins INxP and INxN should be floating (no connection).

1.11 Output Buffer Circuit

The analog output channels are supported using external buffer circuits. A typical buffer circuit is shown in **Figure 4**, comprising current-to-voltage conversion and out-of-band filtering. The typical buffer circuit shown produces a 2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

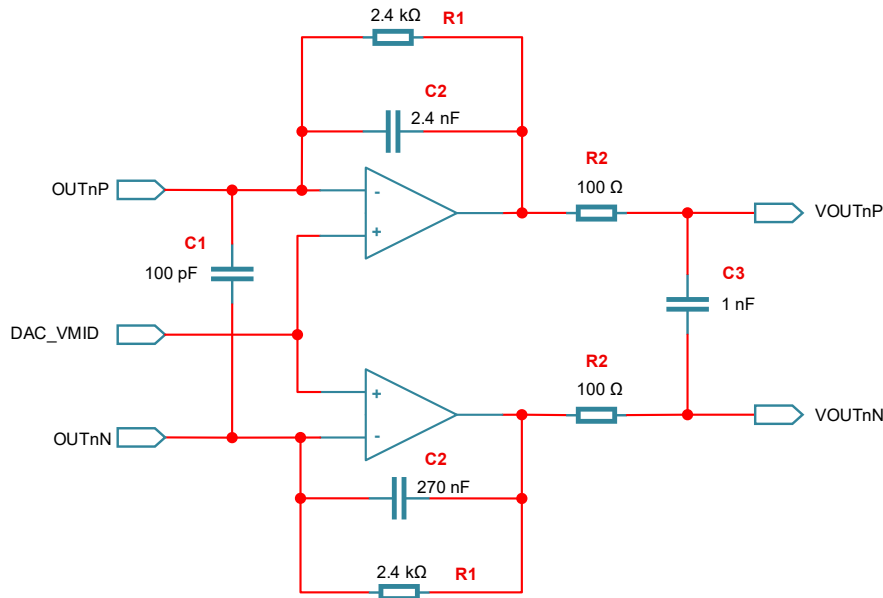


Figure 4: Differential Output Buffer

The full-scale output voltage is determined by the feedback resistor R1. The value of R1 can be calculated using the following equation:

$$R_1(k\Omega) = \frac{\text{Full - scale output voltage } (V_{RMS})}{(\text{Outputs Summed} \times 6.64)}$$

The required value of R1 is shown in Table 8 for a range of typical operating configurations. Note that the THD+N performance may be degraded with increased full-scale output voltage.

Table 8 Feedback Resistor (R1) Selection

Full-Scale Output Voltage		
2 V _{RMS}	4 V _{RMS}	8 V _{RMS}
300 Ω	600 Ω	1.2 kΩ

A low-pass filter is provided using R1 and C2. The filter should be designed to provide a flat passband for the audio bandwidth, while attenuating out-of-band noise. The –3 dB cut-off frequency (F_c) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_1 C_2}$$

The recommended value of C2 is shown in Table 9 for different values of R1. The recommended configuration provides a –3 dB cut-off around 220 Hz.

Table 9 Feedback Capacitor (C2) Selection

Resistor	Capacitor	-3 dB Cutoff
1.2 kΩ	620 pF	214 kHz
600 Ω	1.2 nF	221 kHz
300 Ω	2.4 nF	221 kHz

Additional filtering is provided using R2 and C3. The recommended components attenuate out-of-band noise, while minimizing the capacitive loading on the op-amp device. Using the values shown, the –3 dB cut-off frequency (F_c) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_2 C_3} = \frac{1}{2 \times \pi \times 100 \times 2 \times 1 \times 10^{-9}} = 795.8 \text{ kHz}$$

The DAC_VMID reference is provided as an output from the CS4302P. The DAC_VMID current (arising from capacitor leakage and the output-buffer circuits) must be less than the maximum output current of 10µA. If a larger current is required, an external VMID buffer should be used. See Figure 5 for a buffered DAC_VMID circuit.

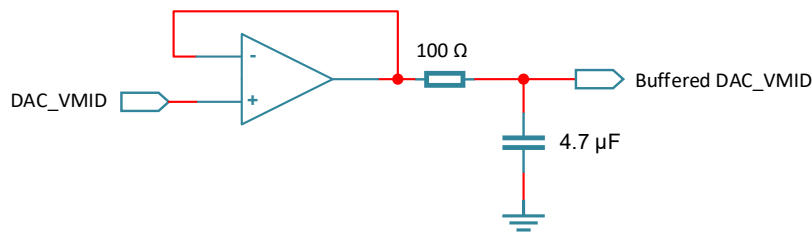


Figure 5 Example DAC_VMID Buffer Circuit

1.11.1 Unused Output Pins

The typical output connection circuit (**Figure 4**) provides a biased differential output. Alternative output buffer circuits may only provide a single-ended output configuration, the unused output pin must be connected to a buffered VMID reference. See for a buffered **Figure 6** VMID circuit.

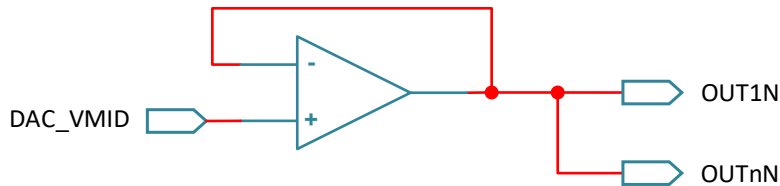


Figure 6: Unused Output pin Connection

1.12 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise op-amps should be used, such as Texas Instruments OP1656. The op-amps should meet the minimum performance requirements noted in **Table 10** Error! Reference source not found.

Table 10 Op-Amp Specification

Parameter	Specification
Input Noise	5 nV/√Hz
Unity Gain bandwidth (G = 1)	15 MHz
Slew Rate	5 V/µs
THD+N	-128 dB

2 General Board Considerations

- Avoid routing digital signals between power planes on an adjacent layer.
- Avoid routing analogue and digital signals next to each other.
- If signals have to cross another signal on an adjacent layer, it is recommend having them cross perpendicular to prevent coupling.
- Signals must not cross power plane shapes and ground cut-offs on an adjacent layer.

3 Layout Guidelines

3.1 Note 1: Digital Signals

- Use controlled 50Ω characteristic impedance for digital signals.

3.2 Note 2: 33R termination Resistors.

- Place Termination resistor close to the device.

3.3 Note 3: Device Decoupling

- Place de-coupling capacitors close to the device.

3.4 Note 4: ADC VMID Decoupling & GND_A pins

- Place de-coupling capacitors close to the device.
- Connect the GND for the VMID capacitors to ground at the closest GND_A pin.
- The GND_A pins should have their own connection to the ground plane and should not be directly connected to the GND paddle.

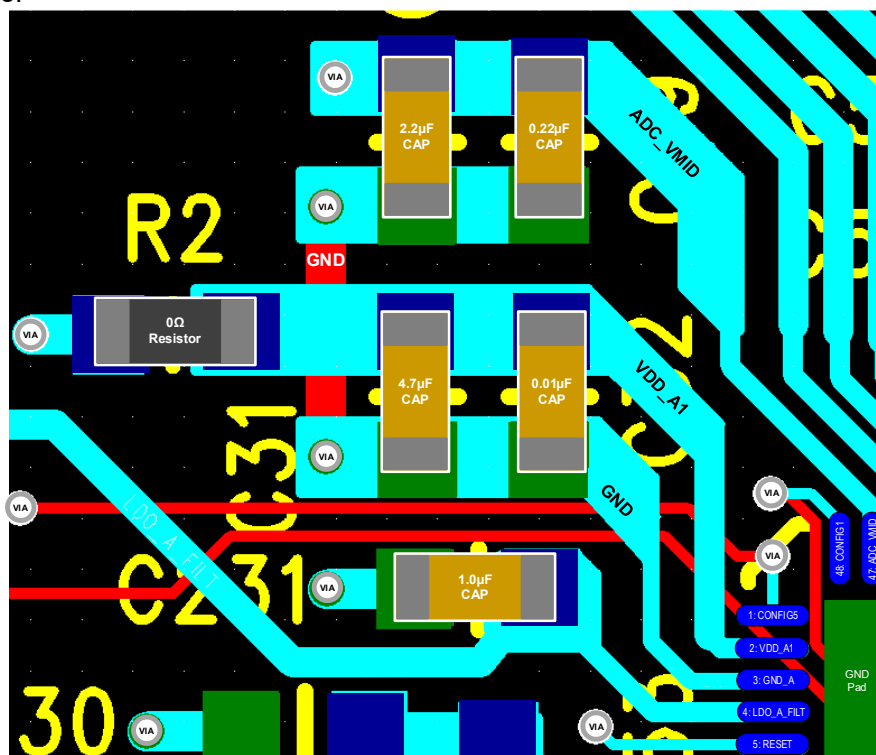


Figure 7: ADC_VMID Decoupling

- Place de-coupling capacitors close to the device.
- Connect the GND for the VMID capacitors to ground at the closest GND_A pin.
- The GND_A pins should have their own connection to the ground plane and should not be directly connected to the GND paddle.

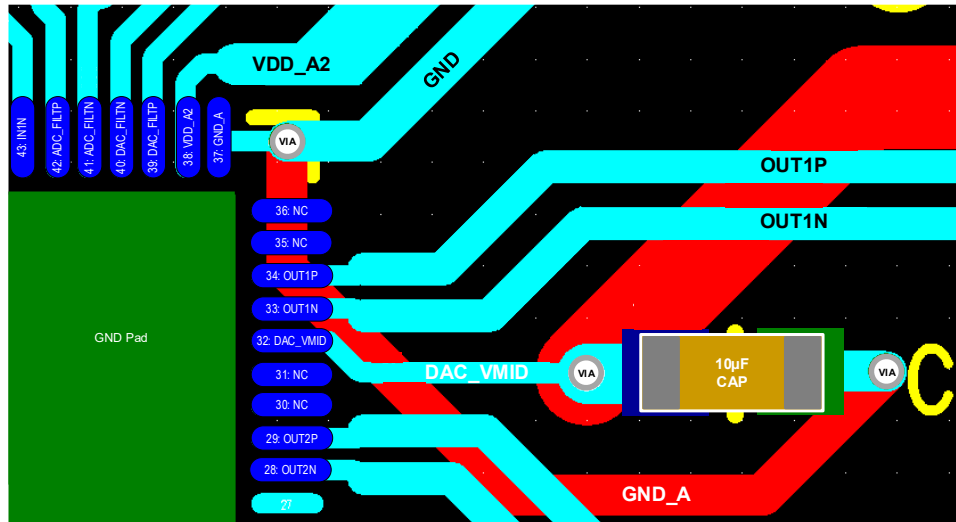


Figure 8: DAC_VMID Decoupling

3.6 Note 6: ADC_FILT Decoupling

- Place de-coupling capacitors close to the device.
- Place the resistor to ground for FILTN between the 2x 470uF capacitors.
- Place the resistor to VDD_A for FILTP between the 2x 470uF capacitors.
- Order of priority for placement of capacitors

Priority		Notes
1	0.47μ	
2	4.7μ	
3	220μ	

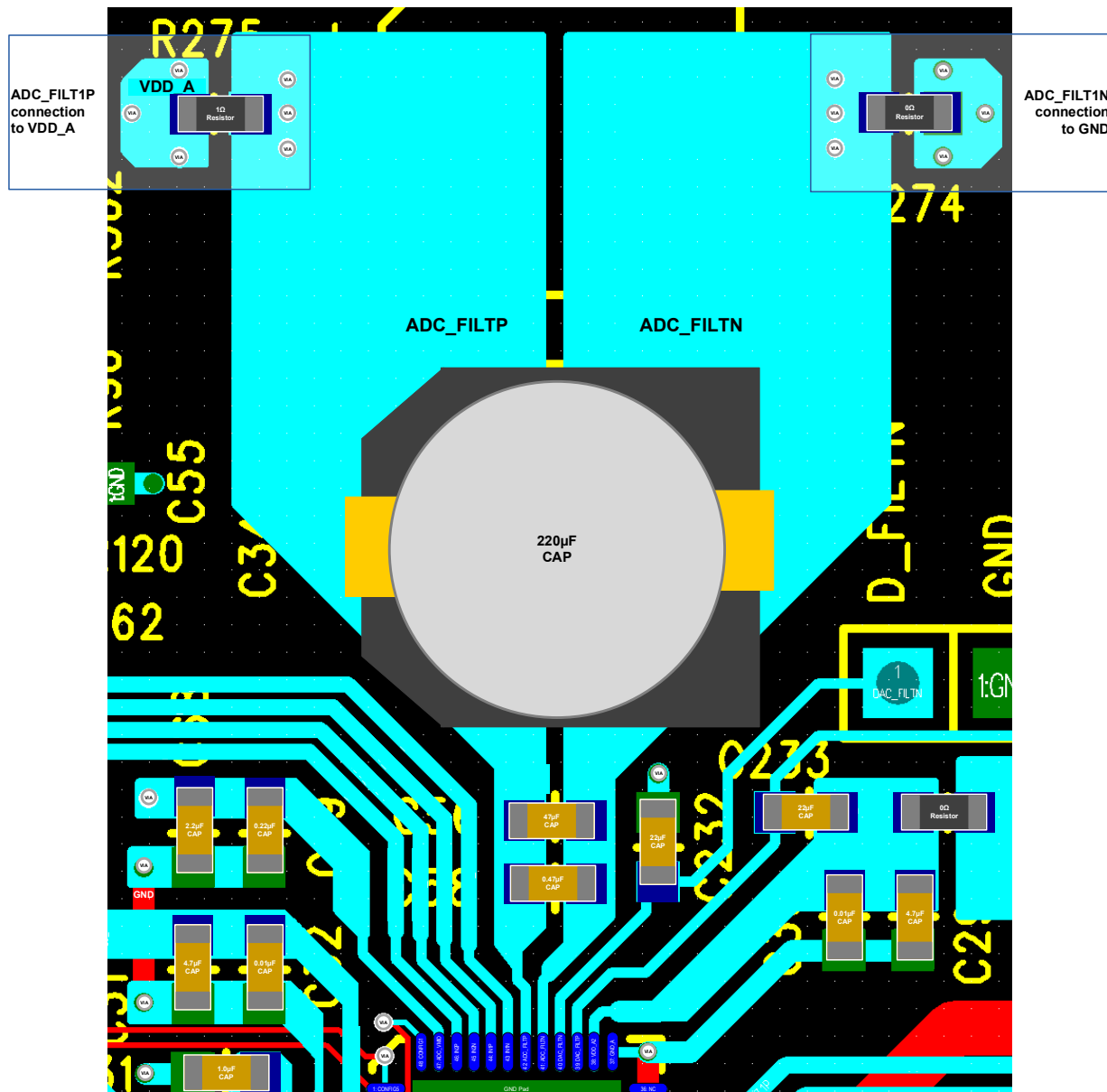


Figure 9: ADC FILTP Decoupling

3.7 Note 7: ADC Input Signal Traces

- To obtain the best performance the DC resistance from the Input Buffer Filters to the ADC input pins should be as low as possible and not exceed 0.5Ω.
- The 1Ω on ADC_INxP/N and 15nF between ADC_INxP/N should be placed as close as possible to the ADC input pins.
- The output signal traces should be routed as a pair with matched length.

Table 11: Signal Track DC resistance for Best Performance

	Min	Typ	Max	Units
DC Resistance			0.5	Ω

3.8 Note 8: DAC_FILT Decoupling

- Place de-coupling capacitors close to the device.
- DAC_FILTP should be connected to VDD_A2 as close as possible to the decoupling capacitors for VDD_A2.

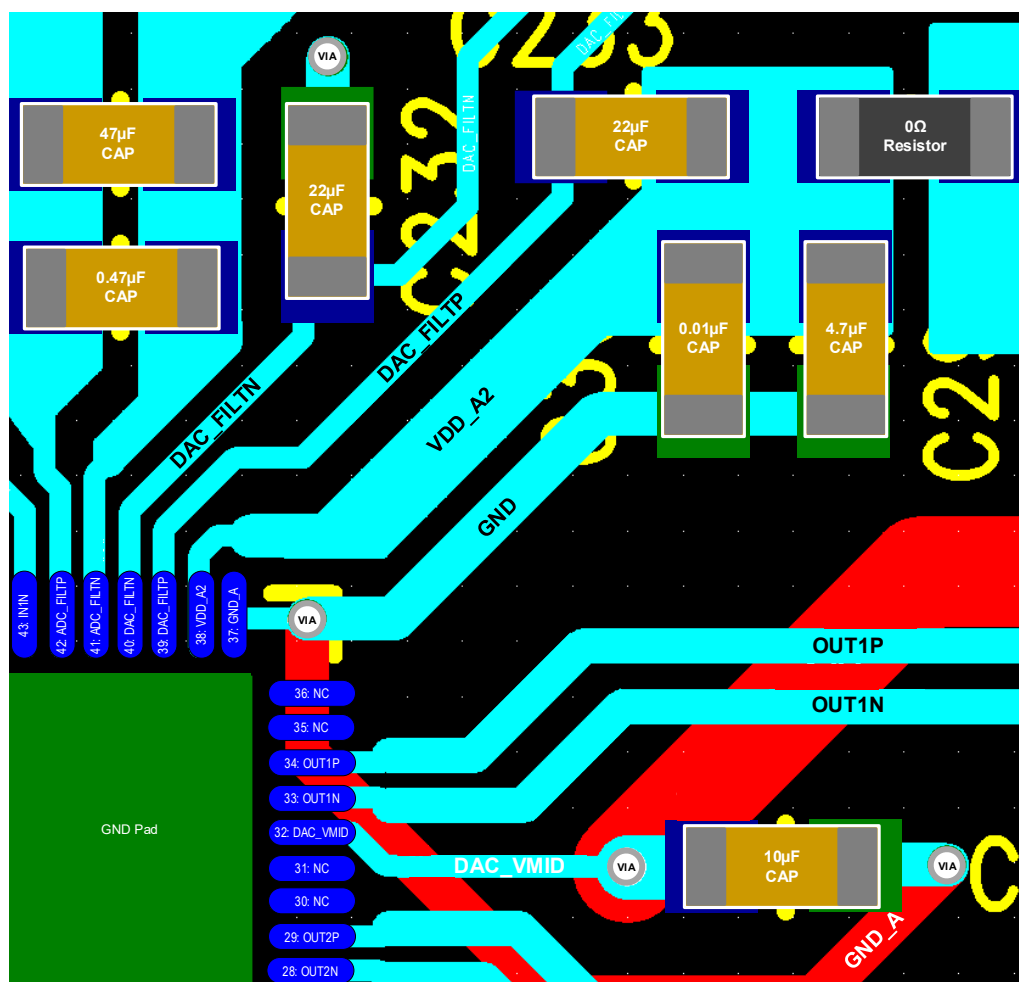


Figure 10: DAC_FILT Decoupling

3.9 Note 8: DAC output pins to I to V Converter Traces

- To obtain the best performance the DC resistance from the DAC output pins to external current to voltage (I to V) converter buffer circuit should be as low as possible and not exceed 0.5Ω.
- The output signal traces should be routed as a pair with matched length.

Table 12: Signal Track DC resistance for Best Performance

	Min	Typ	Max	Units
DC Resistance			0.5	Ω

3.10 Note 10: Ground Cut out.

- The GND_D pin should have its own connection to the ground plane and should not be directly connected to the GND paddle.
- There should be a ground cut-out to help isolate the noisy digital grounds and pins from the analog ground.

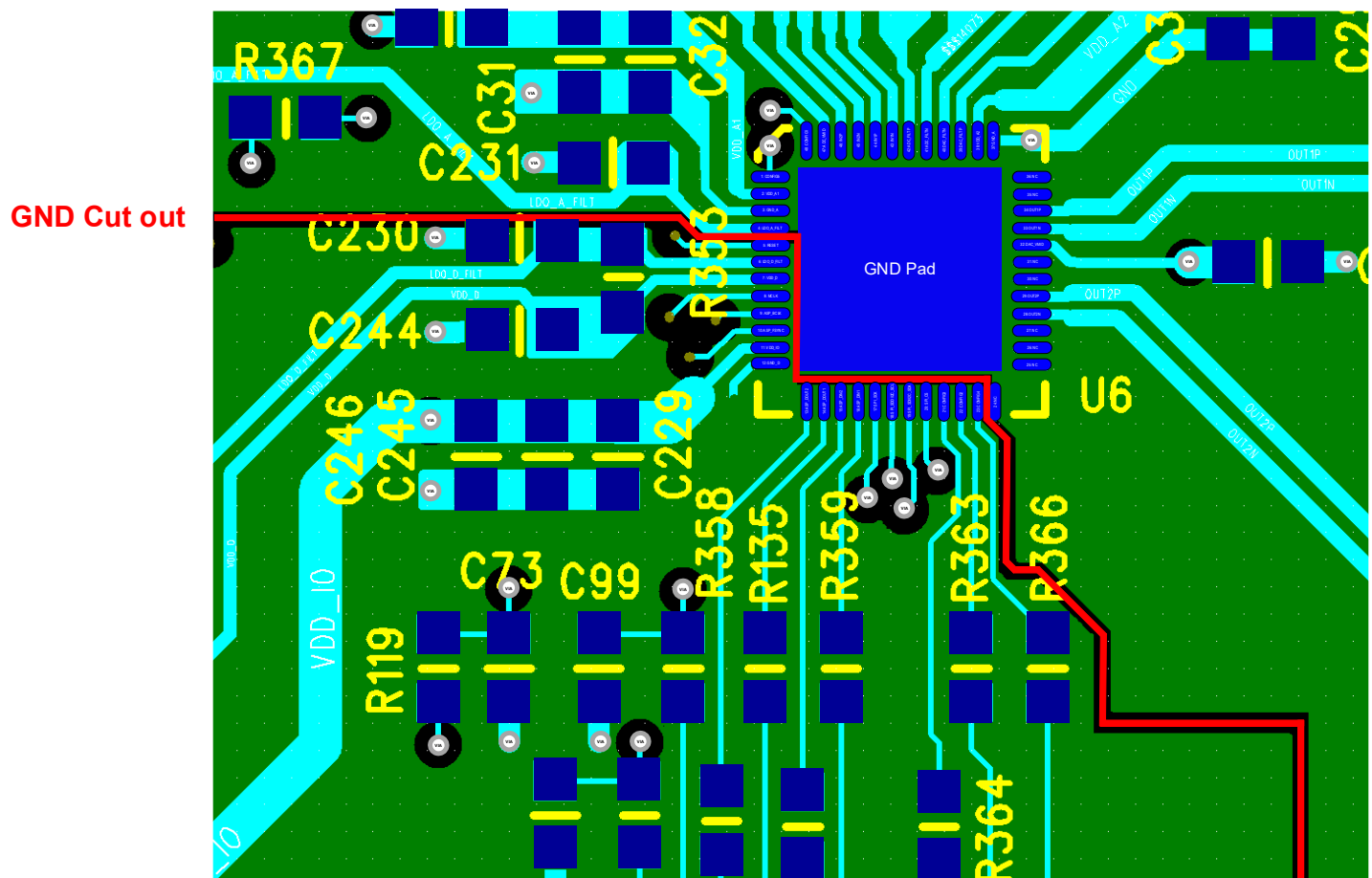


Figure 11: Ground Cut Out on 2nd layer Referenced to Top Layer of DC4302P-DAC Board

4 Revision History

Revision History	
Revision	Changes
7 th July 2025	• Initial version.

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