
CS4302P-DAC Schematic Layout Guidelines

Introduction

This document describes the schematic and layout guidelines for the CS4302P High Performance 2CH Audio DAC.

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1 Recommended External Components

1.1 CS4302P Typical Connection Diagram

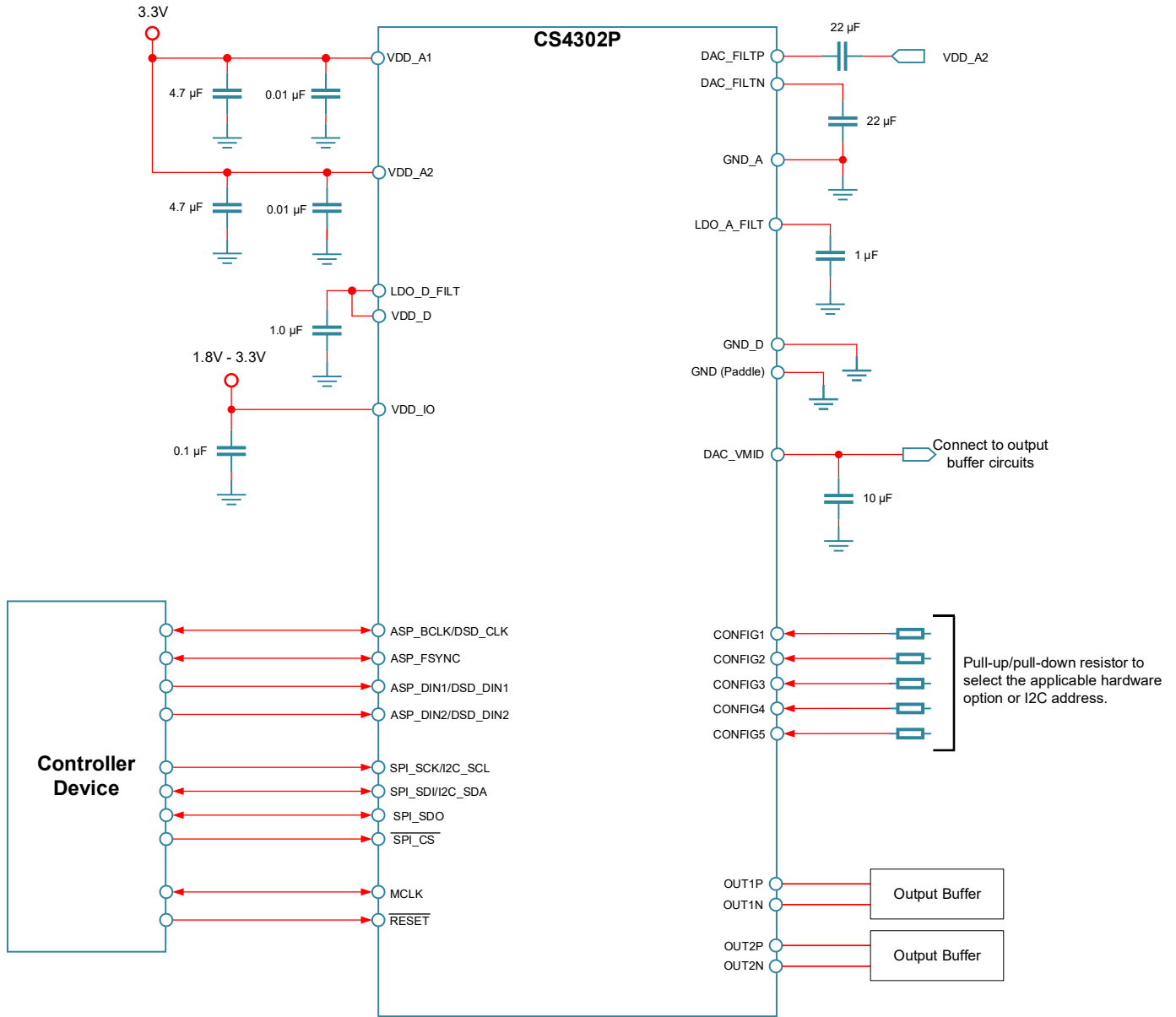


Figure 1: Typical Connection

1.2 I2C Pull-Up

The I2C interface requires pull-up resistor to the VDD_IO supply. The pull-up resistor value is determined by the following factors.

- Bus capacitance
- Minimum I2C drive strength of ICs on the I2C bus

Cirrus Logic recommends the I2C pull-up resistors should be between 2.2k Ω and 10k Ω .

Table 1: i2c Pull-up Resistor

	Min	Typ	Max	Units
I2C pull-up resistors		2.2k to 10k		Ω

1.3 Reset Pull-Up

An optional pull-up resistor to VDD_IO (or pull-down to GND) is only required when the AP/MCU GPIO is unable to drive RESET at all times while the device is powered.

1.4 LDO_A_FILT

The LDO_A_FILT decoupling capacitor must not de-rate to a value less than 0.8 μ F at 1.8V applied to it.

Table 2: LDO_A_FILT Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
1.0 μ F	1.8V	0.8			μ F

1.5 LDO_D_FILT

The LDO_D_FILT decoupling capacitor must not de-rate to a value less than 0.8 μ F at 1.2V applied to it.

Table 3: LDO_D_FILT Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
1.0 μ F	1.2V	0.8			μ F

1.6 DAC_VMID

The DAC_VMID decoupling capacitors should not derate less than minimum value shown in the table below:

Table 4: DAC_VMID Capacitor Derating

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
10 μ F	1.65V	5			μ F

DAC_VMID has a maximum output current of 10 μ A. If the output current (arising from capacitor leakage and the input-buffer circuit) exceeds the maximum output current of the DAC_VMID pin, then an external VMID buffer is required.

1.7 DAC_FILT

The DAC_FILT decoupling capacitors should not derate less than minimum value shown in the table below:

Table 5: DAC_FILT Capacitor Derating Specification

Capacitor Value	Derating Voltage	Min	Typ	Max	Units
22 μ F	3.3V	6.8			μ F

1.8 Output Buffer Circuit

The analog output channels are supported using external buffer circuits. A typical buffer circuit is shown in **Figure 2**, comprising current-to-voltage conversion and out-of-band filtering. The typical buffer circuit shown produces a 2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

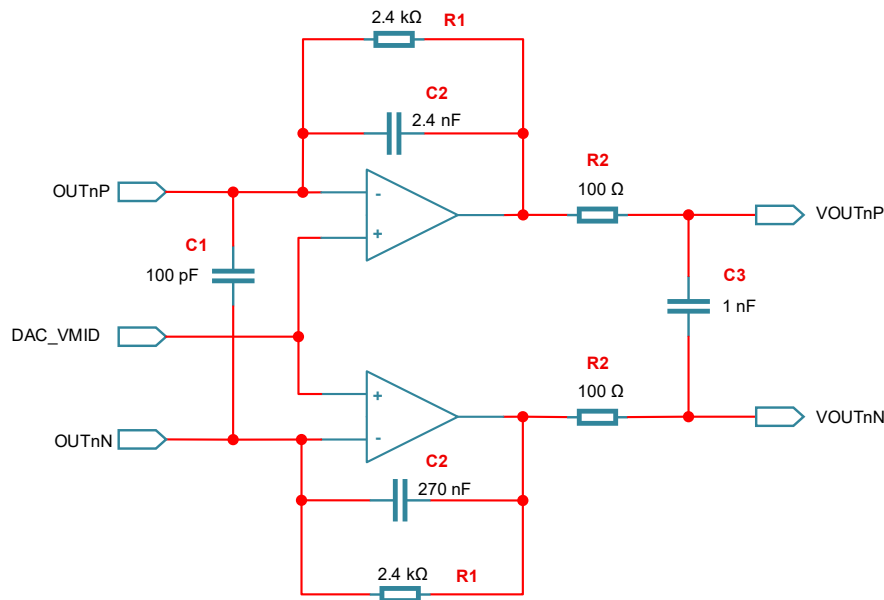


Figure 2: Differential Output Buffer

The full-scale output voltage is determined by the feedback resistor R1. The value of R1 can be calculated using the following equation:

$$R_1(k\Omega) = \frac{\text{Full scale output voltage } (V_{RMS})}{6.64}$$

The required value of R1 is shown in Table 6 for a range of typical operating configurations. Note that the THD+N performance may be degraded with increased full-scale output voltage.

Table 6 Feedback Resistor (R1) Selection
Full-Scale Output Voltage

2 V _{RMS}	4 V _{RMS}	8 V _{RMS}
300 Ω	600 Ω	1.2 kΩ

A low-pass filter is provided using R1 and C2. The filter should be designed to provide a flat passband for the audio bandwidth, while attenuating out-of-band noise. The –3 dB cut-off frequency (F_c) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_1 C_2}$$

The recommended value of C2 is shown in Table 7 for different values of R1. The recommended configuration provides a –3 dB cut-off around 220 Hz.

Table 7 Feedback Capacitor (C2) Selection

Resistor	Capacitor	-3 dB Cutoff
1.2 kΩ	620 pF	214 kHz
600 Ω	1.2 nF	221 kHz
300 Ω	2.4 nF	221 kHz

Additional filtering is provided using R2 and C3. The recommended components attenuate out-of-band noise, while minimizing the capacitive loading on the op-amp device. Using the values shown, the –3 dB cut-off frequency (F_c) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_2 C_3} = \frac{1}{2 \times \pi \times 100 \times 2 \times 1 \times 10^{-9}} = 795.8 \text{ kHz}$$

The DAC_VMID reference is provided as an output from the CS4302P. The DAC_VMID current (arising from capacitor leakage and the output-buffer circuits) must be less than the maximum output current of 10μA. If a larger current is required, an external VMID buffer should be used. See Figure 3 for a buffered DAC_VMID circuit.

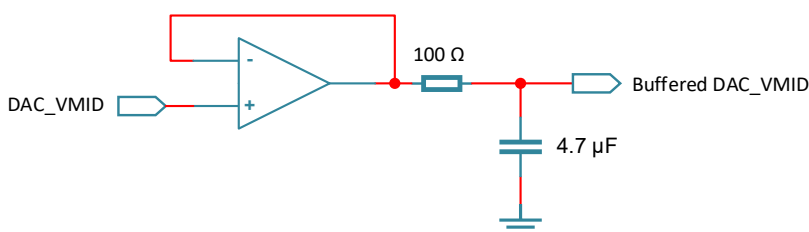


Figure 3 Example DAC_VMID Buffer Circuit

1.8.1 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise op-amps should be used, such as Texas Instruments OP1656. The op-amps should meet the minimum performance requirements noted in Table 8

Table 8 Op-Amp Specification

Parameter	Specification
Input Noise	5 nV/√Hz
Unity Gain bandwidth ($G = 1$)	15 MHz
Slew Rate	5 V/μs
THD+N	-128 dB

1.8.2 Unused Output Pins

The recommended output buffer circuit (Figure 2) provides a differential connection to the output pins OUTxP and OUTxN. Alternative output-buffer circuits may use only a single-ended connection to OUTxP or OUTxN. If a single-ended output configuration is used, the unused output pin must be connected to a buffered DAC_VMID reference. See Figure 4 or a buffered DAC_VMID circuit.

If one or more output channel is not used (disabled), the respective output pins OUTxP and OUTxN should be floating (no connection).

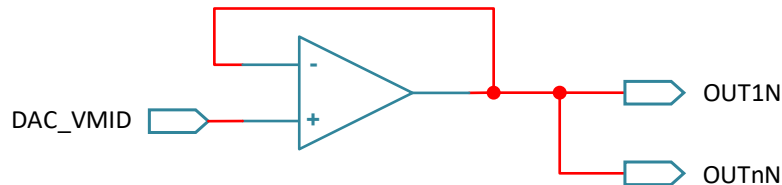


Figure 4: Unused Output pin Connection

2 General Board Considerations

- Avoid routing digital signals between power planes on an adjacent layer.
- Avoid routing analogue and digital signals next to each other.
- If signals have to cross another signal on an adjacent layer, it is recommend having them cross perpendicular to prevent coupling.
- Signals must not cross power plane shapes and ground cut-offs on an adjacent layer.

3 Layout Guidelines

3.1 Note 1: Digital Signals

- Use controlled 50Ω characteristic impedance for digital signals.

3.2 Note 2: 33R termination Resistors.

- Place Termination resistor close to the device.

3.3 Note 3: Device Decoupling

- Place de-coupling capacitors close to the device.

3.4 Note 4: VMID Decoupling & GND_A pins

- Place de-coupling capacitors close to the device.
- Connect the GND for the VMID capacitors to ground at the closest GND_A pin.
- The GND_A pins should have their own connection to the ground plane and should not be directly connected to the GND paddle.

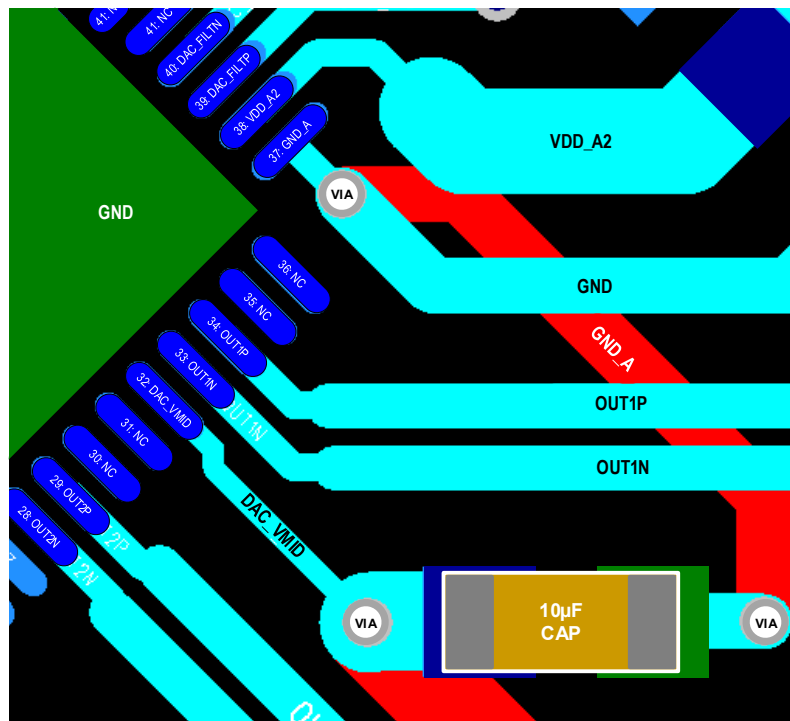
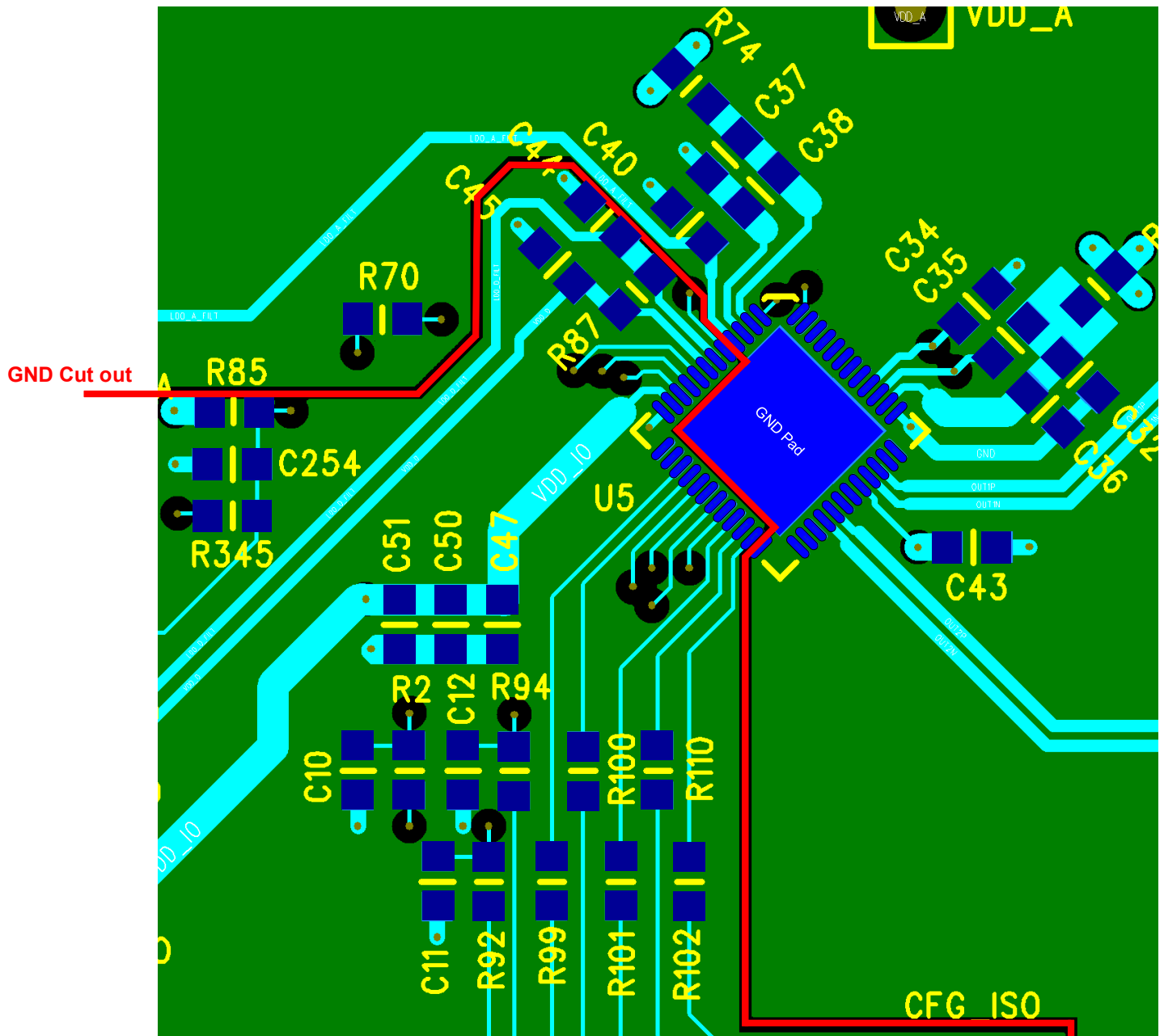


Figure 5: VMID Decoupling

3.7 Note 7: Ground Cut out.

- The GND_D pin should have its own connection to the ground plane and should not be directly connected to the GND paddle.
- There should be a ground cut-out to help isolate the noisy digital grounds and pins from the analog ground.



4 Revision History

Revision History	
Revision	Changes
8 th JUL 2025	• Initial version.

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