

DESIGN AND EVALUATION OF AN AUDIO DAC WITH NON-UNIFORMLY WEIGHTED DYNAMIC ELEMENT MATCHING

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A new dynamic element matching scheme for very high performance audio DACs has been developed. The elements have binary weighted values that allow increased resolution at the multi-bit sigma-delta output without requiring an excessive number of elements. This has allowed a low order multi-bit sigma-delta modulator to be used with the result of low out of band noise. A new evaluation test has been employed to compare the performance of this architecture with existing architectures.

INTRODUCTION

The first delta-sigma modulator based audio DACs were predominately single bit designs. The reason for this was that with only two levels to implement, any errors in the reproduced DAC levels manifest as gain and offset errors and do not affect the linearity and noise performance of the overall system. Having only two levels provides very coarse quantisation for an audio signal with the result that most of the power in the output signal is unwanted noise which needs to be filtered out after the DAC.

Whilst it is extremely difficult to make a 16-24 bit non-delta-sigma DAC, one advantage of such an approach is the low out of band noise. However if such a DAC operates at a low rate (approaching the Nyquist rate for the signal) e.g., 44.1kHz and 48kHz for audio signals, the output spectrum will contain strong image components. The solution to this is to use an interpolating filter to increase the sample rate without significant images.

More recently it has become common to combine delta-sigma modulation with a multi-level DAC with a modest number of output levels to provide an improvement in out of band noise and signal images. Out of band energy is undesirable since it can result in audio band components due to non-linearity in the system at high frequencies. A typical audio DAC system is shown in Figure 1.

The PCM input signal has its sample rate increased using an interpolation filter that attenuates the image components. The high sample rate signal is then delta-sigma modulated to reduce the number of levels used. This introduces additional quantisation noise, but the operation of the delta-sigma modulator feedback loop ensures that very little additional noise is introduced over the audio bandwidth. If the delta-sigma modulator produces a single one-bit output signal, this may then be fed directly into a one bit DAC. However it is better to retain a few bits of resolution at the delta-sigma output to reduce the out of band noise.

If a regular multi-bit DAC is used, any errors in the reproduced analogue levels contribute to in-band noise and distortion placing unrealisable tolerances on the analogue components. To overcome this, further processing of the multi-bit signal is performed to decompose it into a number of individually delta-sigma modulated signals, the sum of which provides the output. This process is called dynamic element matching (DEM) since it lessens the required matching accuracy of the DAC elements [Norsworthy]. Each of these signals has the characteristics of single bit delta-sigma modulated signal. The two level DEM system outputs are used to control how DAC elements are selected. The combination of a two-level signal and DAC element may be considered to be a two-level DAC. The output of the complete DAC system is then the sum of all the two-level DAC outputs.

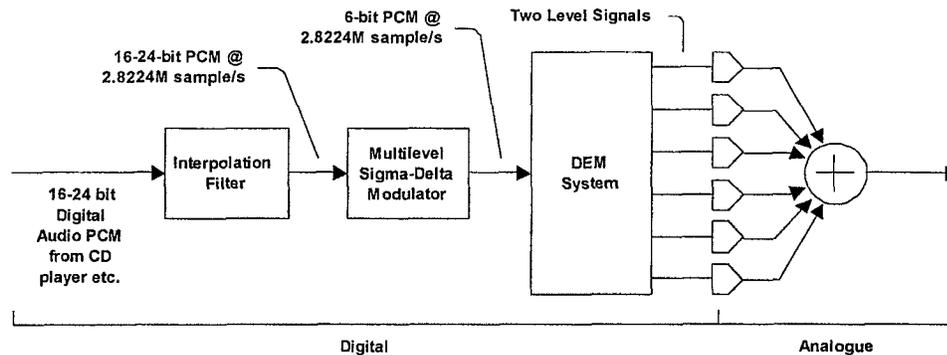


Figure 1 Audio DAC System

Most such multi-level DAC schemes employ equally weighted unit elements. For example, a five-bit converter will have 31 or 32 unit elements. The dynamic element matching (DEM) schemes that are commonly used only work for equally weighted elements.

This limits the number of bits before the number of individually controlled unit elements becomes unmanageable. A method for increasing the number of DAC levels without significantly increasing the number of controlling signals is described here.

DYNAMIC ELEMENT MATCHING (DEM)

The idea behind all dynamic element matching techniques is to decompose a digital input sequence into a number of output sequences which are used to drive multiple DACs whose outputs are summed to provide an analogue output (Figure 1). The sum of these output sequences is always equal to the input sequence at every sample instant. Each output signal can take on only two levels which are used to determine how a particular DAC element is used (either use / not use or use in a positive / negative sense). The two level output signals are arranged to have a frequency spectrum that has little power at low frequencies other than that associated with the input signal. This results in reduced errors at low frequencies when the DAC elements have errors from their nominal values. In particular, linearity is improved since particular DAC elements are not used predominately for any particular set of input values - each DAC element is used with approximate equal frequency as any other in the system, for any input sequence.

A simple scheme for DEM is to always use the elements that have not been used for the longest period. Equivalently, the elements are used cyclically, so that

for code n , the next n elements are used - for the next sample, say code m , the next m elements in the cycle after the ones that have just been used for code n are used. This ensures that on average each element is used equally often for whatever input codes. For DC signals, this system is perfectly linear even if there are errors in the values of the elements. It can be shown that the error is shaped in the frequency domain with first order shaping with a zero at DC [Henderson]. The effect of errors is reduced at low frequencies, but not eliminated. Since the error is only shaped by a first order function there are similar concerns as for first order delta-sigma modulators - in particular the presence of in-band tones for small DC offsets. This scheme is only applicable to equally weighted DAC elements.

DEM WITH NON-EQUALLY WEIGHTED ELEMENTS

The DEM block used in the WM8740 decomposes the input samples consisting of 6 bit PCM words into 14 individual one-bit delta-sigma modulated outputs. (If equally weighted elements had been used, this would require at least 63 outputs to represent codes between 0 and 63 making layout less practical.)

The weighted sum of the 14 outputs always equals the input code plus an offset. The weights used are 2 x one unit, 2 x two units, 2 x four units and 8 x eight units giving a total of 78 switched units. To provide an offset to move potential tones away from the small signal region, an additional two-unit capacitor is used which always contributes in a positive sense. This offset is easily compensated for by adding an opposite offset to the input.

The decomposition from 6 bit PCM into the vector output is performed in stages. The first stage examines the LSB of the input. If the LSB is zero, then it is necessary that the two one-unit elements are used in

opposite senses so as to cancel – there is a choice as to which is driven high and which is driven low. If the LSB is one, it is then necessary that both one-unit elements are used in the same sense – there is a choice as to whether they are both driven high, or both driven low. The one-unit elements are driven in this way to ensure that on subtracting their contribution from the input the result is always an even number. Since the remainder is known to be even, the LSB can be ignored so the remainder has one fewer bit of word-length than the input. By cascading stages it is possible to successively peel-off LSBs. The final remainder can be fed into a more conventional DEM block to process the final data.

Each stage uses a vector delta-sigma modulator [Schreier & Zhang]. In this case two delta-sigma loops are used in each stage and the two modulators are coupled together using a vector quantiser. The vector quantiser has an input to indicate whether an odd or even total output is required. The inputs to each of the delta-sigma modulators are zero – this then causes the output signal to have a zero mean. Thus the overall DEM input signal is not present on the outputs of each DEM stage, except for the last one. The action of the loop filters ensures that each individual output has little power at low frequencies so that mismatches between the elements results in little change in the in-band signal.

Random number sequences are used in the DEM stages to randomise the decisions which are made to reduce the likelihood of repetitive patterns being generated in the outputs. Additionally dither is added in before the multilevel re-quantiser in the second order delta sigma modulator which drives the DEM stage. The hardware cost for each stage is very low – 2 D-type latches and a few adders and other gates.

DAC ARCHITECTURE

The DAC is configured as a switched capacitor filter to further reduce out of band noise. Another advantage of the multi-level DAC and filter combination is that the output has minimal change from sample to sample – this reduces the sensitivity to clock jitter.

EVALUATION OF DAC

Measured results from the DAC are shown in Figures 2 and 3. Figure 2 shows that the noise floor is consistently low for all inputs. For large signals a small amount of distortion is present. Figure 3 shows the wide-band output spectrum at the device outputs without any off-chip filtering. This shows the performance of the WM8740 in comparison to a sigma-delta DAC from another supplier. Here the benefit of reduced out of band noise from the use of a low order multi-bit DAC is readily apparent. Additionally, the images around 8Fs (384kHz) are seen to be much reduced due to the use of a linear interpolator rather than a sample-and-hold.

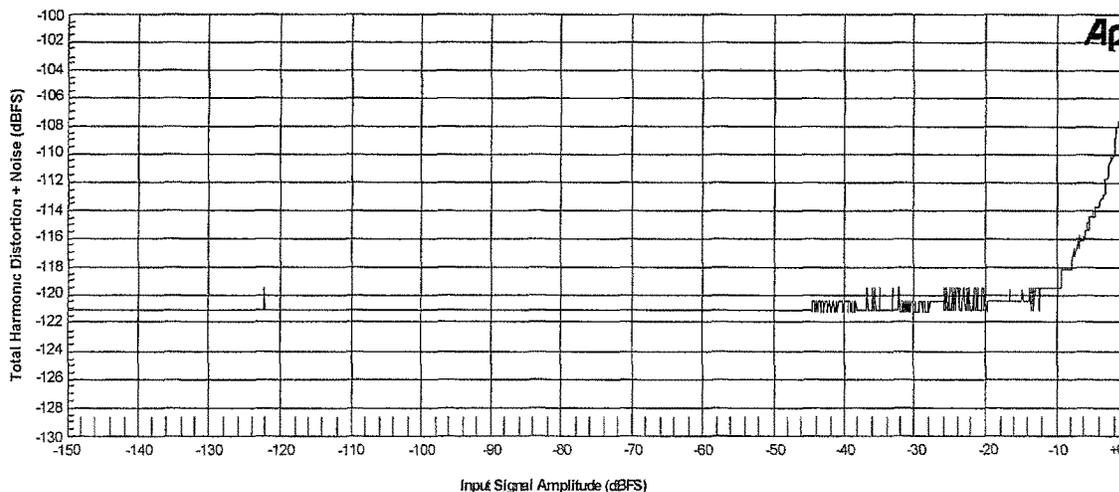


Figure 2. WM8740 Audio DAC Performance

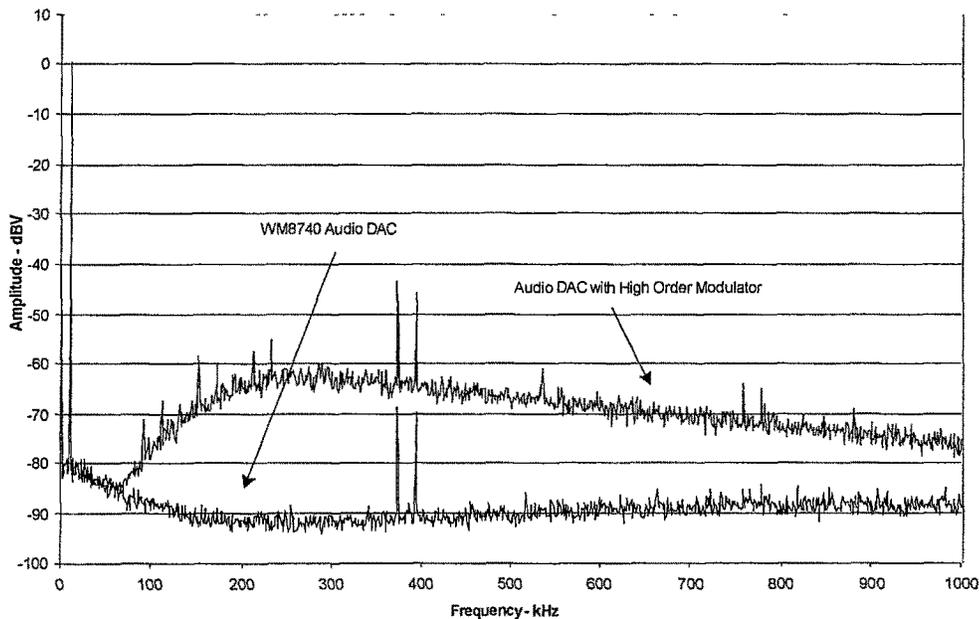


Figure 3. WM8740 Output Spectrum versus High Order Modulator Output Spectrum

Typically audio DAC specifications include signal to noise + distortion (SINAD) for a full-scale signal, and the dynamic range (measured for a -60dB input signal). These individual numbers cannot be extrapolated to determine the performance for other input signals and do not give any indication of whether the error is correlated to the signal (harmonics), or has noise-like properties, or is concentrated at certain frequencies unrelated to the desired signal frequency (tones). Ideally the error signal should be noise-like with characteristics which do not change with input signal. Tonal type errors must be avoided since the ear is particularly adept at picking out tones from background noise.

A graph of background noise versus swept AC level can indicate tonal problems if the background noise level varies. Most papers on DEM contain many plots of SNR versus signal level. Often these graphs show that most of the degradation occurs for input levels around -60dB . However these plots do not give any indication as to *why* this should occur. However by using a DC sweep to first identify regions of the input range which have poorer noise, it is possible to track down and improve or eliminate these sources of noise

DC SWEEP TEST

Rather than sweeping AC amplitude, it is more illuminating to sweep the DC level slowly and to measure the in-band AC noise power. Ideally this will be a flat line indicating that the noise characteristics are independent of the signal level. However in the presence of element matching error, significant peaks will occur around certain DC levels, effectively giving a “signature” of the particular type of dynamic element matching used and the effectiveness of any dithering applied.

Having identified regions of poorer performance, either by simulation or measurement, steps can be taken to improve the performance. Often there is a region around mid-scale where the performance can be significantly degraded due to cycling patterns forming either in the delta-sigma modulator or in the DEM system. This can be seen by considering the effect of a small DC input. With no DC input, the modulator may idle between two codes e.g. 0,1,0,1,0,1 etc. When a small positive DC offset is introduced, additional 1s must appear in the sequence occasionally. If the DC offset is small enough and the system not randomised enough by dither, then it is likely that the additional 1's

will appear at almost regular intervals giving rise to a tone. If the DC level is increased the additional 1's will appear more often causing the tone to rise in frequency, and also power level. Further increases in DC level cause the tone frequency to go outside the measurement bandwidth (usually 20kHz) with the result that the in-band noise/tone power improves. This phenomenon occurs symmetrically giving a pair of noisy regions that are centred on mid-scale. The performance degradation that is often seen at around -60dB is due to this effect – at this level the peaks of the sinusoidal signal fall in the regions with poor performance. Larger signals occupy less time in the noisy regions and smaller signals lie in the null between the pair of noisy regions around mid-scale. As these noisy regions are typically less than one percent of full scale, small signal performance can be improved by deliberately applying a small DC offset at the input to the DAC and removing this DC offset in the analogue domain. Obviously if the input source happens to have an opposite DC offset, then this modification will actually degrade performance, but digital audio sources usually have any offsets removed.

A similar argument applies to the standard rotating DEM scheme with a component mismatch. A small DC offset causes the element selection pattern to slowly rotate and with a component mismatch a low frequency tone can occur. Again this may be alleviated by use of a DC offset, dither or higher order modulation.

The in-band noise modulation test can be quite time consuming. Many hundreds or even thousands of points are necessary to be sure of catching all of the very narrow features. Thus this method is appropriate for device evaluation and characterisation and not for production test. It is also very suitable for comparing different DEM methods and the effects of dither by simulation. Equivalent testing techniques may be applied to delta-sigma ADCs with similar benefits.

Figure 4 shows the result of this DC sweep for the WM8740. This is very flat, with very small peaks visible. This should be compared with Figure 5, a sigma-delta DAC from another supplier.

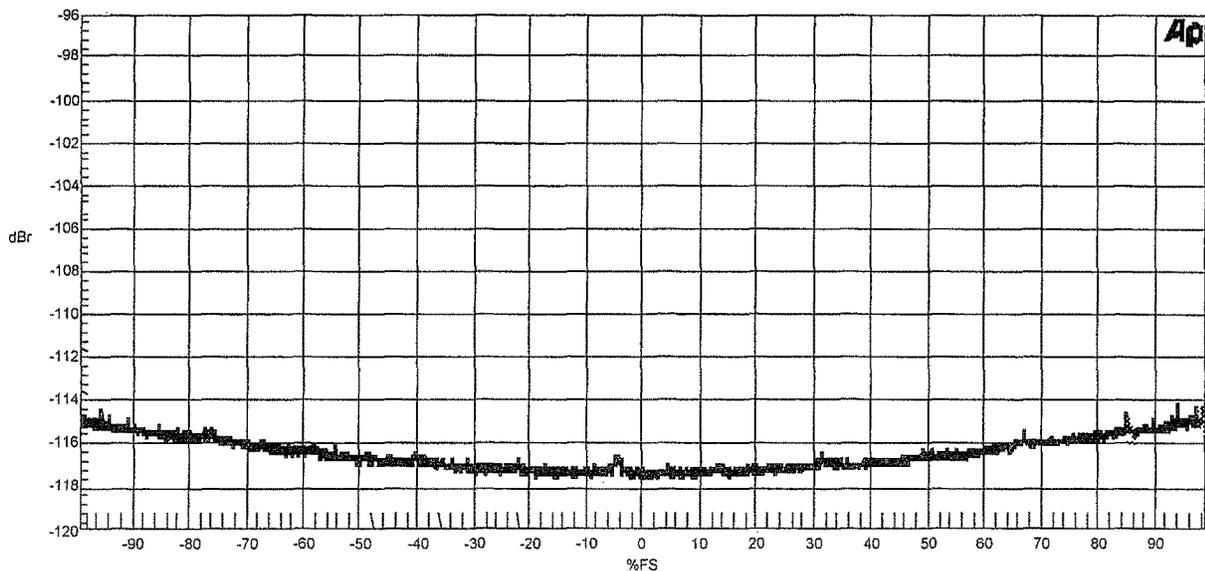


Figure 4. DC Offset Test – WM8740

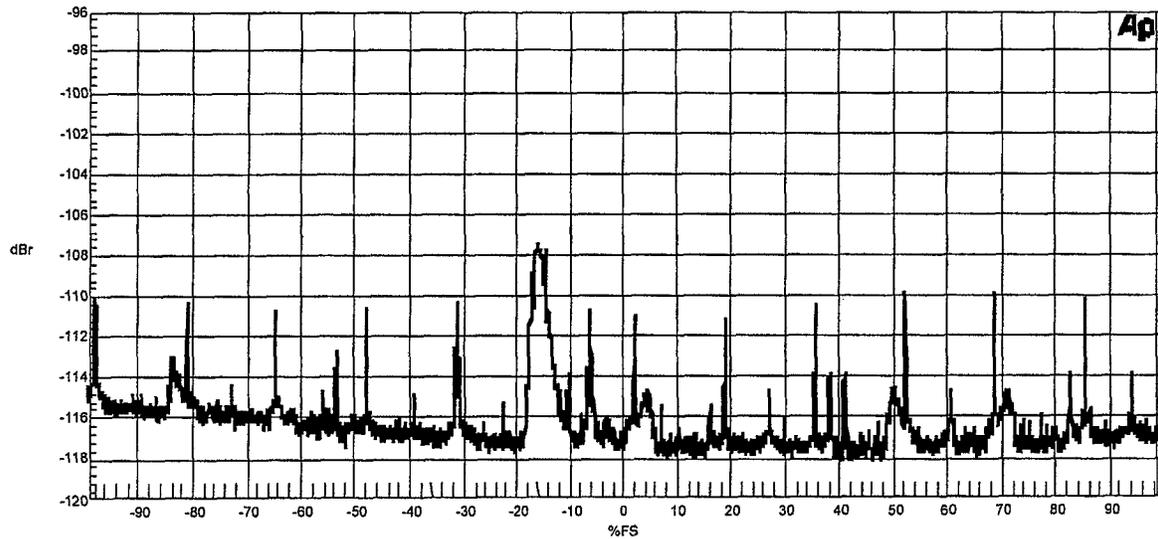


Figure 5. DC Offset Test – A Competitor's "117dB" DAC

CONCLUSIONS

A high performance audio DAC exploiting a new DEM method has been designed and implemented on silicon. This method has been shown to have advantages in out-of-band noise and in superior in-band noise modulation. Using a DC sweep test it is possible to characterise the dependency on the input signal for the noise and tonal power. It is preferable that the noise power does not change with input level and the DAC described here achieves this.

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