WM8524 Recommended Power Sequence

INTRODUCTION

The WM8524 $2V_{RMS}$ DAC features ground referenced outputs and a DC servo to effectively eliminate power on pops and clicks.

The recommended power on/off sequence is very simple to implement, but there are a number of timing constraints that need to be followed to ensure the best possible performance.

These timing constraints will also be important in calculating if optimum power down pop performance can be achieved in emergency power down situations.

This document also stipulates the power-up to audio out timing, detailed in the recommended power on sequence section.

RECOMMENDED POWER ON SEQUENCE

1) To power up the device, apply AVDD and LINEVDD.
2) Wait for VMID to rise to V_{pord_hi} and for AVDD/LINEVDD to rise above V_{pora_hi} and settle. These timings will be dependent on the system design - see Table 2 for V_{pord_hi} and V_{pora_hi} typical voltage levels.
3) Start MCLK and BCLK and set $\overline{MUTE}$ =1. The device will be ready to output audio Δt after a logical AND of MCLK, BCLK, $\overline{MUTE}$ and $\overline{POR}$, as shown in Figure 1.

See Table 1 for Δt Power up to audio out timing – this is dependent on the sampling rate and MCLK frequency.

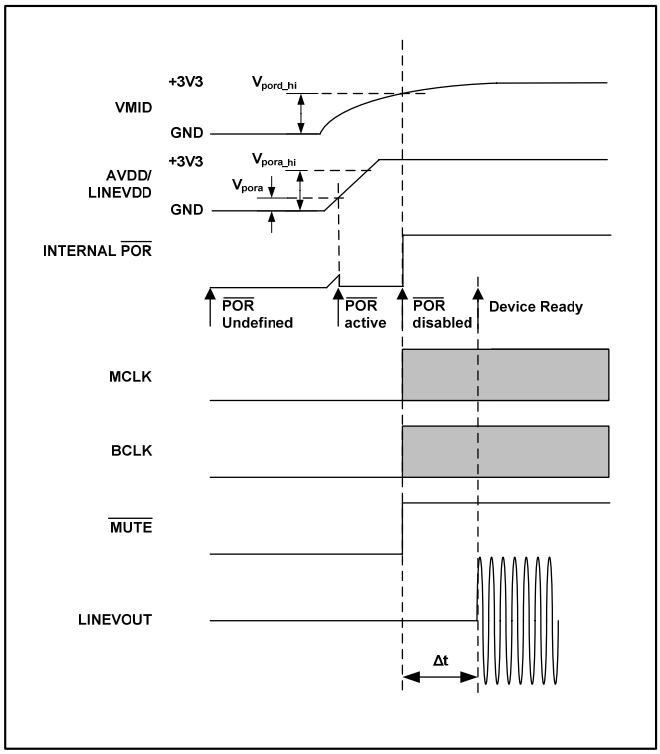

Figure 1 – Recommended Power-up sequence timing

SAMPLING RATE (LRCLK) (KHZ)	Δt POWER UP TO AUDIO OUT TIMING (ms)						
	128fs	**192fs**	**256fs**	**384fs**	**512fs**	**768fs**	**1152fs**
8	Unavailable	Unavailable	965	1003	849	502	481
11.025	Unavailable	Unavailable	700	728	616	365	350
16	Unavailable	Unavailable	483	502	425	252	241
22.05	Unavailable	Unavailable	351	365	309	183	176
32	Unavailable	Unavailable	242	252	213	127	121
44.1	Unavailable	Unavailable	176	183	155	92	Unavailable
48	Unavailable	Unavailable	162	168	143	85	Unavailable
88.2	239	263	89	92	Unavailable	Unavailable	Unavailable
96	220	241	82	85	Unavailable	Unavailable	Unavailable
176.4	120	132	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192	111	121	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 1 - Power up to audio out timing

Test Conditions

LINEVDD = AVDD = 3.3V AGND = LINEGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (LINEVDD/AVDD rising)	V_{pora}	Measured from LINEGND		158		mV
VDD level to POR rising edge (VMID rising)	V_{pord_hi}	Measured from LINEGND	0.63	0.8	1	V
VDD level to POR rising edge (LINEVDD/AVDD rising)	V_{pora_hi}	Measured from LINEGND	1.44	1.8	2.18	V
VDD level to POR falling edge (LINEVDD/AVDD falling)	V_{pora_lo}	Measured from LINEGND	0.96	1.46	1.97	V

Table 2 Power on Reset

Note: All values are simulated results

RECOMMENDED POWER OFF SEQUENCE

1) Set $\overline{\text{MUTE}}$ =0
2) Wait for shutdown time Δs (See Table 3)
3) Remove MCLK, AVDD and LINEVDD

Ensure that during the shutdown time (Δs) the BCLK and LRCLK are left running for 800 samples to allow the soft mute to assert fully. See **Figure 2** for the timing diagram.

Note that in emergency shutdown situations (such as supply voltages collapsing) the shutdown must be completed before the $\overline{\text{POR}}$ is asserted to ensure best pop/click performance. This timing will be dependent on the system design - see Table 2 for V_{pora_lo} typical level.

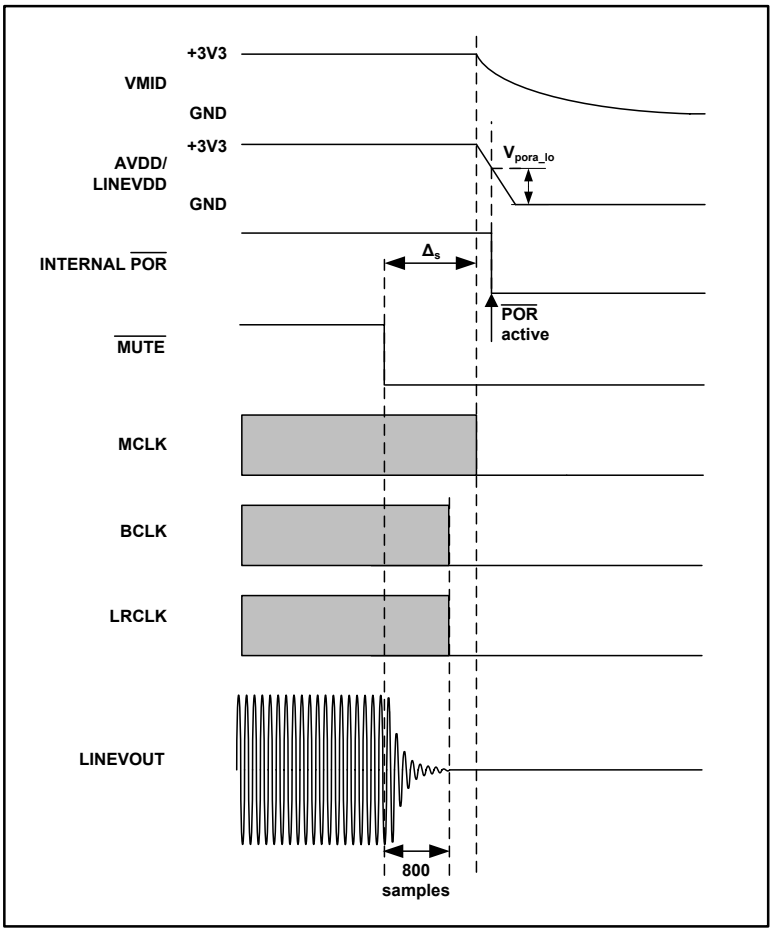

Figure 2 - Recommended Power-down sequence timing

SAMPLING RATE (LRCLK) (KHZ)	Δs SHUTDOWN TIME (ms)						
	128FS	192FS	256FS	384FS	512FS	768FS	1152FS
8	Unavailable	Unavailable	693	731	577	422	422
11.025	Unavailable	Unavailable	504	532	420	307	307
16	Unavailable	Unavailable	349	368	291	213	213
22.05	Unavailable	Unavailable	254	268	212	156	156
32	Unavailable	Unavailable	177	186	148	109	109
44.1	Unavailable	Unavailable	129	136	108	80	Unavailable
48	Unavailable	Unavailable	91	96	77	59	Unavailable
88.2	183	183	67	70	Unavailable	Unavailable	Unavailable
96	168	168	67	70	Unavailable	Unavailable	Unavailable
176.4	94	94	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192	86	86	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 3 - Δs shutdown time

CONCLUSION

By following the timing constraints set out in this document, the customer can implement the optimum power up/down pop and click performance.

The customer can also calculate how long the device will take to power-up to audio out in their application, and how long the device will take to power down before it is safe to remove signals and power.

APPLICATION SUPPORT

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